

FACULTY of Computer Science and Management / DEPARTMENT					
SUBJECT CARD					
Name in Polish: Architektury Komputerów Równoległych					
Name in English: Parallel Computer Architecture					
Main field of study (if applicable): Informatics					
Specialization (if applicable): Computer Engineering					
Level and form of studies: 1st/ 2nd* level, full-time / part-time*					
Kind of subject: obligatory / optional / university-wide*					
Subject code INZ0143Wcs					
Group of courses YES /NO*					
	Lecture	Classes	Laboratory	Project	Seminar
Number of hours of organized classes in University (ZZU)	30	15			15
Number of hours of total student workload (CNPS)	90	60			60
Form of crediting	Examination / crediting with grade*				
For group of courses mark (X) final course	X				
Number of ECTS points	3	2			2
including number of ECTS points for practical (P) classes					
including number of ECTS points for direct teacher-student contact (BK) classes	1,8	1,2			1,2

*delete as applicable

PREREQUISITES RELATING TO KNOWLEDGE, SKILLS AND OTHER COMPETENCES

1. Basic knowledge of computer architecture and organization
2. Basic skills in programming

SUBJECT OBJECTIVES

- C1 Acquainting students with extend knowledge related to parallel computer architectures
- C2 Acquainting students with different ways of parallel program execution
- C3 Acquainting students with architecture of currently produced microprocessors and parallel computers
- C4 Acquisition of the ability to choose the most suitable parallel architecture to the solved problem
- C5 Acquisition of the ability of evaluation of used processor architecture

SUBJECT EDUCATIONAL EFFECTS

relating to knowledge:

PEK_W01 He has extended knowledge related to parallel computers architectures

PEK_W02 He knows different ways in which parallel program execution can be performed

PEK_W03 He knows different architecture of currently produced microprocessors and computers

relating to skills:

PEK_U01 He is able to choose parallel environment to the selected problem

PEK_U02 He is able to evaluate the processor architecture

PROGRAMME CONTENT

Form of classes - lecture		Number of hours
Lec 1	Fundamentals of Computer Design. Technology Trends. Taxonomy of parallel computers. Harvard, Princeton and Harvard-Princeton architectures	2
Lec 2	Instruction level parallelism. Data dependences and hazards. Dynamics Scheduling – the idea. Dynamic Scheduling using Tomasulo’s Approach	2
Lec 3	Delay branch. Basic branch predictions schema. Branch target buffers.	2
Lec 4	Multiple issue processors. Hardware based speculation. Limitation of Instruction Level parallelism.	2
Lec 5	Basic compilers techniques for exploiting Instruction Level Parallelism	2
Lec 6	Multiprocessor and thread level parallelism. Symmetric shared-memory and distributed shared-memory	2
Lec 7	Evaluations of parallel systems: performance metrics, scalability of parallel systems, Amdhal and other laws. Granularity concept.	2
Lec 8	Models of memory consistency	2
Lec 9	Pipeline processors, identification of conflicts and it's avoiding	2
Lec 10	Vector processors and vectorization process	2
Lec 11	Clusters as a parallel computers	2
Lec 12	Architecture of GPU. CUDA and OpenCL.	2
Lec 13	Hybrid Message Passing/Shared Memory Computers.	2
Lec14	Non-conventional way of processing - dataflow computers	2
Lec15	New trends in computer architecture	
	Total hours	30
Form of classes - class		Number of hours
Cl 1	Presentation of classes scope and grading principles. Solving simple problems related with parallel execution .	1
Cl 2	Data dependences and hazards analysis	2
Cl 3	Dynamic Scheduling using Tomasulo’s Approach	2

CI 4	Evaluation of branch prediction algorithms	2
CI 5	Automatic reordering of program execution. Program execution with speculation	2
CI 6	Exploiting of Instruction Level Parallelism	2
CI 7	Evaluations of parallel systems	2
CI 8	Models of memory consistency	2
	Total hours	15
Form of classes - laboratory		Number of hours
Lab1		
Lab2		
...		
	Total hours	
Form of classes - project		Number of hours
Proj1		
Proj2		
...		
	Total hours	
Form of classes - seminar		Number of hours
Sem1	Presentation of the classes scope and grading principles . Rules related to student presentations. Determining the schedule of student presentations.	1
Sem2 – Sem8	During seminar will be presented architecture of currently produced microprocessors and parallel computers. The specific architectures that will be presented will be selected for each edition of the course on the basis of current knowledge of microprocessors and parallel computers producers.	14
	Total hours	15
TEACHING TOOLS USED		
N1. Lecture supported by multimedia presentations (slideshow)		
N2. Seminars supported by multimedia presentations (slideshow)		
N3. Classes supported by blackboard		

EVALUATION OF SUBJECT EDUCATIONAL EFFECTS ACHIEVEMENT

Evaluation(F – forming (during semester), P – concluding (at semester end)	Educational effect number	Way of evaluating educational effect achievement
F1 – (lecture)	PEK_W01 PEK_W02	Quizzes during the lecture, student activity during the lecture, students answering on questions during lecture
F2 – (class)	PEK_U01 PEK_U02	Quizzes during the classes, student activity during the classes, assessment of students solutions presented during

		classes (points allocated).
F3 – (seminar)	PEK_W03	Evaluation of the presentation at the seminar and prepared documentation from the presentation. The evaluation shall be subject to the fulfillment of the requirements for the presentation, including its substantive scope, structure and organization. Participation in the discussions after presentation is also evaluated.

P - the final assessment will be issued on the basis of partial grades (points) received from the final exam (E) and the evaluation of F1, F2, F3 as follows:

$$\text{Grade} = 40\% * E + 10\% * F1 + 25\% * F2 + 25\% * F3$$

In order to receive a positive grade from each activity is required to obtain at least 40% of the points.

PRIMARY AND SECONDARY LITERATURE

PRIMARY LITERATURE:

- [1] V. Kumar i inni, "Introduction to Parallel Computing", The Benjamin/Cummings Pub., New York 2003.
- [2] J D. Patterson, J. Hennessy, "Computer Architecture – a Quantitative Approach", Elsevier
- [3] D. Patterson, J. Hennessy, Computer Organization and design, Elsevier
- [4] A.Y.H. Zomaya, „Parallel and distributed computing handbook”, McGraw-Hill, New York 1996 B. Wilkinson, M. Allen, "Parallel Programming, Prentice Hall, 2005

SECONDARY LITERATURE:

- [1] Technical documentation available on the Web related to MIPS, Intel and AMD processors

SUBJECT SUPERVISOR (NAME AND SURNAME, E-MAIL ADDRESS)

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MATRIX OF CORRELATION BETWEEN EDUCATIONAL EFFECTS FOR SUBJECT
Parallel Computer Architecture
AND EDUCATIONAL EFFECTS FOR MAIN FIELD OF STUDY **Informatics**
AND SPECIALIZATION **Computer Engineering**

Subject educational effect	Correlation between subject educational effect and educational effects defined for main field of study and specialization (if applicable)**	Subject objectives***	Programme content***	Teaching tool number***
PEK_W01 (knowledge)	K2INF_W06	C1	Lec1, Lec7, Lec8, Lec9, Lec10, Lec11, Lec12, Lec13, Lec14, Lec15	N1
PEK_W02	K2INF_W06	C2	Lec2, Lec3, Lec4, Lec5, Lec6, Lec7, Lec12	N1
PEK_W03	K2INF_W06	C3	Sem1 – Sem8	N2
PEK_U01 (skills)	K2INF_U08	C4	C11 – C18	N3
PEK_U02	K2INF_U08	C5	C11 – C18	N3

** - enter symbols for main-field-of-study/specialization educational effects

*** - from table above